

FDMJ1028N

N-Channel 2.5V Specified PowerTrench® MOSFET

20V, 3.2A, 90mΩ

Features

- Max $r_{DS(on)}$ = 90mΩ at V_{GS} = 4.5V
- Max $r_{DS(on)}$ = 130mΩ at V_{GS} = 2.5V
- Low gate charge
- High performance trench technology for extremely low $r_{DS(on)}$
- RoHS Compliant

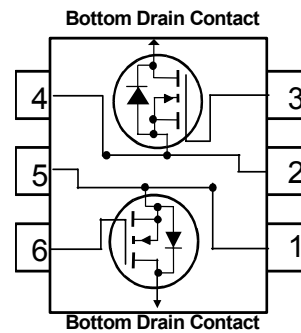
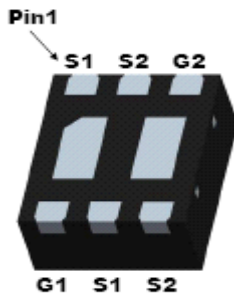


General Description

This dual N-Channel 2.5V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. The $r_{DS(on)}$ and thermal properties of the device are optimized for battery power management applications.

Applications

- Battery management
- Baseband Switches



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	±12	V
I_D	Drain Current -Continuous	3.2	A
	-Pulsed	12	
P_D	Power Dissipation for Single Operation	(Note 1a)	W
		(Note 1b)	
T_J, T_{STG}	Operating and Storage Temperature	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	89	°C/W
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Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
028	FDMJ1028N	7"	8mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		13		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16, V_{GS} = 0\text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	0.6	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		-3		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5\text{V}, I_D = 3.2\text{A}$		76	90	m Ω
		$V_{GS} = 2.5\text{V}, I_D = 2.5\text{A}$		106	130	
		$V_{GS} = 4.5\text{V}, I_D = 3.2\text{A}, T_J = 125^\circ\text{C}$		89	132	
g_{FS}	Forward Transconductance	$V_{GS} = 5\text{V}, I_D = 3.2\text{A}$		7.5		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		200		pF
C_{oss}	Output Capacitance			50		pF
C_{rss}	Reverse Transfer Capacitance			30		pF
R_G	Gate Resistance		$f = 1\text{MHz}$		1	

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{V}, I_D = 1\text{A}, V_{GS} = 4.5\text{V}, R_{GS} = 6\Omega$		7	14	ns
t_r	Rise Time			8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			11	20	ns
t_f	Fall Time			2	4	ns
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DD} = 15\text{V}, V_{GS} = 3.2\text{V}, V_{GS} = 4.5\text{V}$		2	3	nC
Q_{gs}	Gate to Source Gate Charge			0.4		nC
Q_{gd}	Gate to Drain Charge			1.0		nC

Drain-Source Diode Characteristics

V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 1.16\text{A}$		0.8	1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 3.2\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$		11		ns
Q_{rr}	Diode Reverse Recovery Charge			2.5		nC

Notes

1: $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5×1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $89^\circ\text{C}/\text{W}$ when mounted on a 1in^2 pad of 2 oz copper



b. $156^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2: Pulse Test: Pulse Width < $3000\mu\text{s}$, Duty Cycle < 2.0%

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

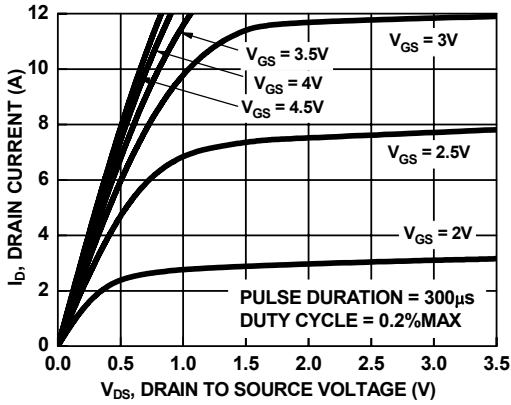


Figure 1. On Region Characteristics

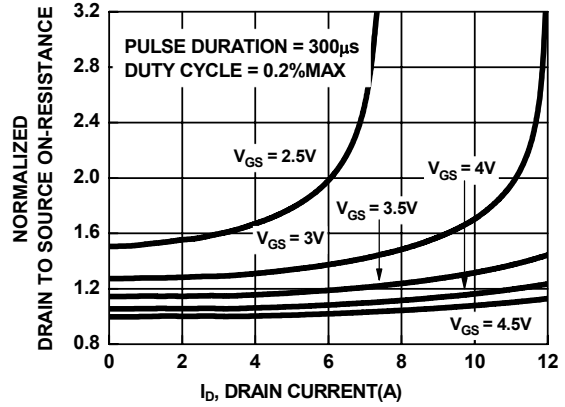


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

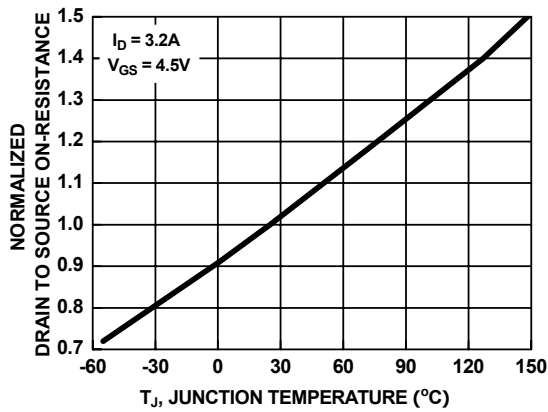


Figure 3. Normalized On Resistance vs Junction Temperature

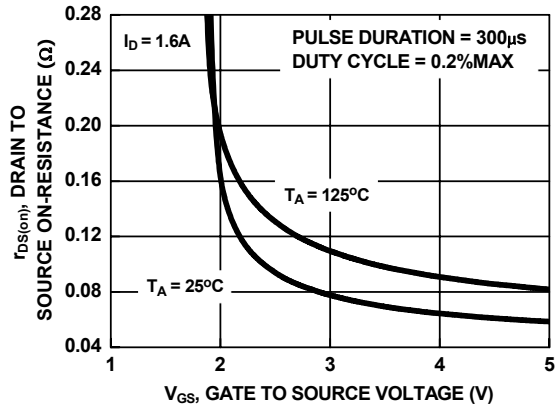


Figure 4. On-Resistance vs Gate to Source Voltage

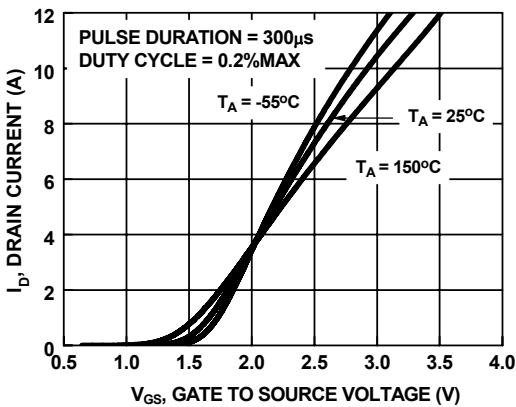


Figure 5. Transfer Characteristics

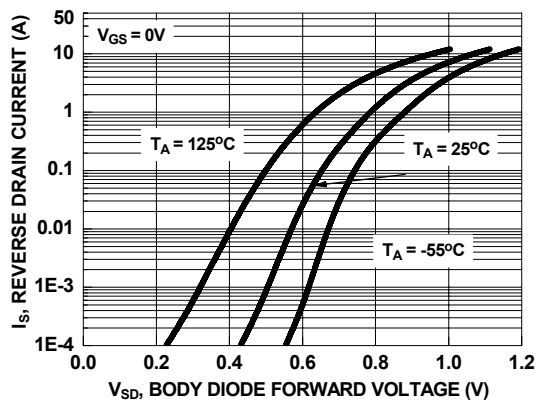


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

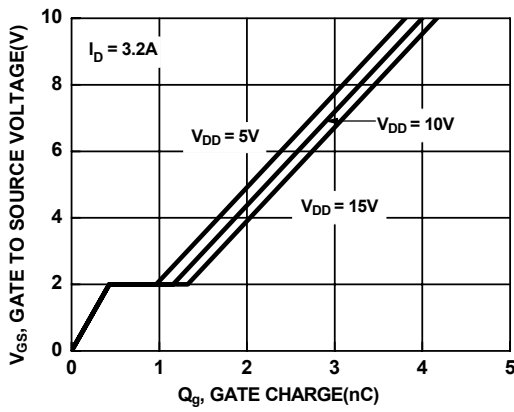


Figure 7. Gate Charge Characteristics

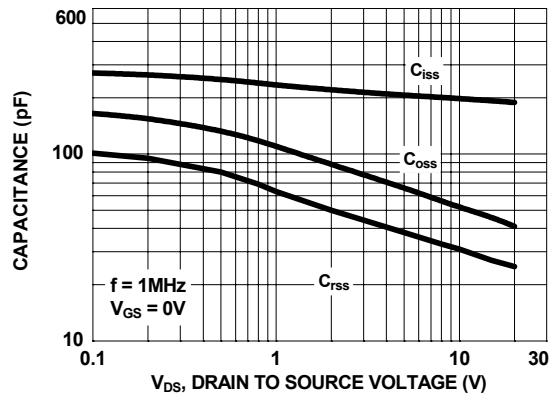


Figure 8. Capacitance vs Drain to Source Voltage

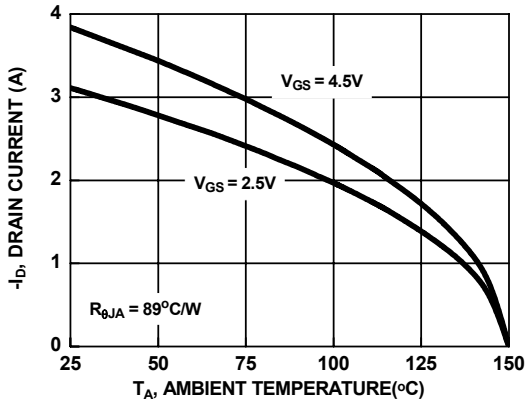


Figure 9. Maximum Continuous Drain Current vs Ambient Temperature

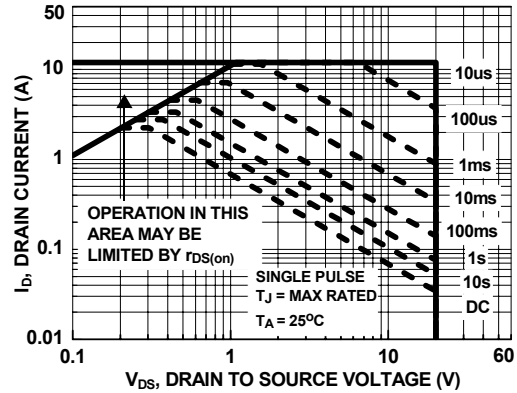


Figure 10. Forward Bias Safe Operating Area

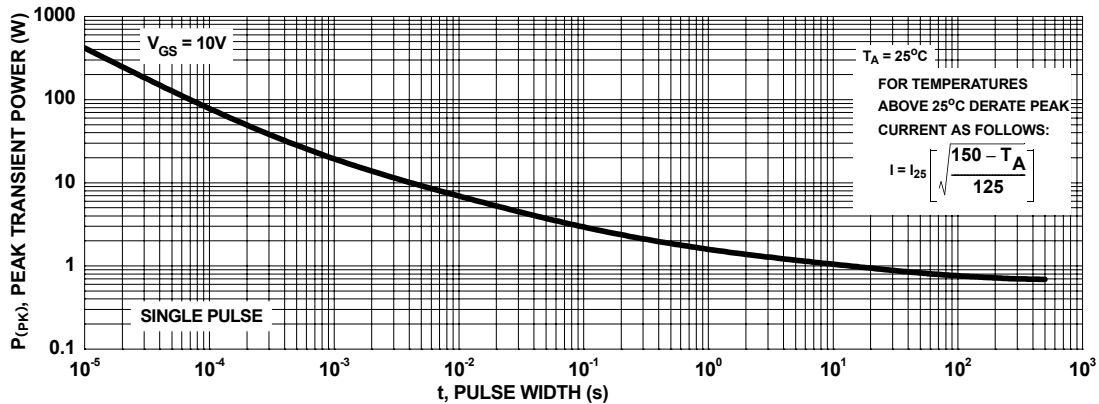


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

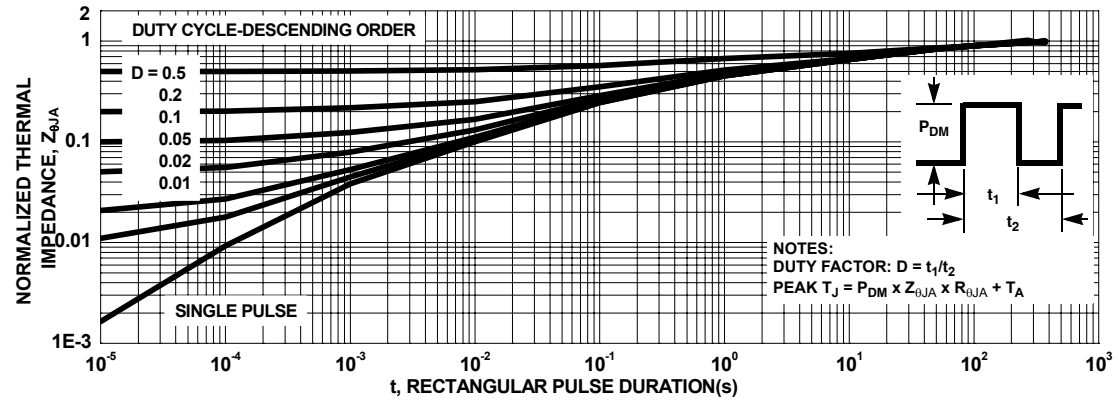
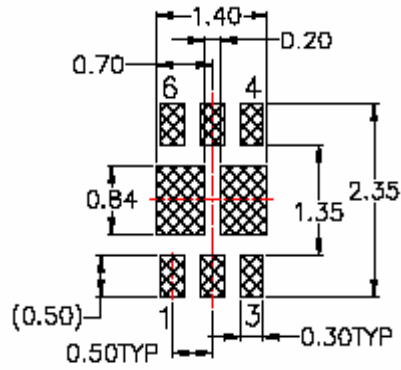
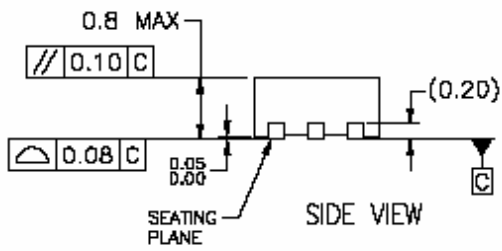
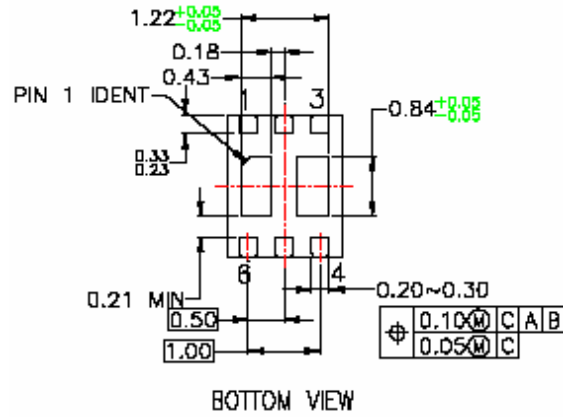
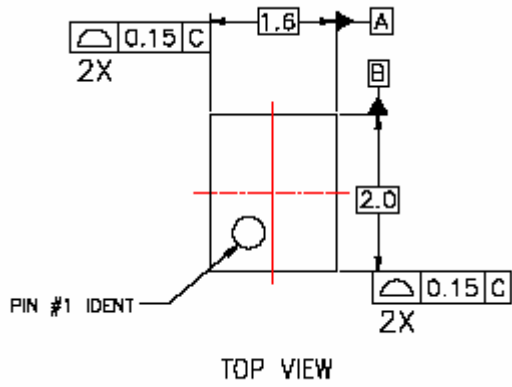


Figure 12. Transient Thermal Response Curve

Dimensional Outline and Pad Layout



RECOMMENDED LAND PATTERN

NOTES:

- A. NON JEDEC REGISTRATION MOLDED PACKAGE OUTLINE,
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994

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Rev. 119